CLAIMS

1. An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register configured to store coordinates of a pixel to be drawn on the display;

a calculation circuit configured to calculate an address of a location in a memory for storage of data corresponding to said pixel; and

a control circuit configured to control said register and said calculation circuit to cause said data to be written to and stored in said memory at said address.

2. The apparatus as claimed in claim 1, wherein said memory comprises a first register configured to store an X coordinate of said pixel and a second register configured to store a Y coordinate of said pixel.

3. The apparatus as claimed in claim 1, further comprising:

a clipping circuit for comparing said X and Y coordinates with predetermined clipping limits and generating a clipping signal configured to indicate clipping of said X and Y coordinates.

4. The apparatus as claimed in claim 3, wherein said control circuit is further configured to control writing of said data to said address in said memory, in response to said clipping signal.

5. The apparatus as claimed in claim 3, wherein said control circuit is further configured to control the calculation of said address in said memory in response to said clipping signal.

6. The apparatus as claimed in claim 3, wherein said clipping circuit and said calculation circuit are further configured to calculate said address and cause said data to be written to and stored at said address in said memory when said X and Y coordinates fall within said

predetermined clipping limits and not calculate said address when said X and Y coordinates fall outside said predetermined clipping limits.

7. The apparatus as claimed in claim 2, wherein said first register is memory mapped to a first and a second location in said memory and said second register is memory mapped to a third and a fourth location in said memory.

SUBA2T

8. The apparatus as claimed in claim 7, wherein said apparatus further comprises:

an address decoder for monitoring said first, second, third and fourth memory locations and applying a location signal to said control circuit representative of an address location being written to.

9. The apparatus as claimed in claim 8, wherein said control circuit is further configured to control said first and second registers and said calculation circuit, in response to a receipt of said location signal from said address decoder

10. The apparatus as claimed in claim 9, wherein said control circuit is further configured to instruct said calculate circuit to calculate said address for a pixel coordinate in response to one of the following:

a X coordinate being sent to the first register at a preselected one of said first and second locations; and

a Y coordinate being sent to the second register at a preselected one of said third and fourth locations.

11. An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register for storing coordinates of a pixel to be drawn;

a calculation circuit for receiving said coordinates from said register and calculating an address of a location in a memory for storage of data corresponding to said pixel in dependance on said coordinates;

a control circuit for controlling said register and said calculation circuit to cause said data to be written to and stored in said memory at said address;

a style table for storing data corresponding to a predetermined pattern or style for said pixel to be drawn; and

a style counter for indexing said data in said style table and generating a style data signal corresponding to said indexed data.

12. The apparatus as claimed in claim 11, wherein said style table is large enough to store the longest non-repeating bit pattern required for a drawing operation.

13. The apparatus as claimed in claim 11, wherein said style table is large enough to store the longest non-repeating bit pattern required for a drawing operation.

14. The apparatus as claimed in claim 13, wherein said first register is memory mapped to a first to fourth location group in said memory and said second register is memory mapped to a fifth to eighth location group in said memory; and

said apparatus further comprising an address decoder for monitoring said first to further and said fifth to eighth location groups applying a location signal to said control circuit representative of an address location being written to and indexing said style counter in response to the address location being written to.

15. An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register for storing coordinates of a pixel to be drawn on said display;

a calculation circuit for receiving said coordinates from said register and calculating an address of a location in a memory for storage of data corresponding to said pixel in response to said coordinates; and

a control circuit for controlling said register and said calculation circuit to cause said data to be written to and stored in said memory at said address, wherein said calculation circuit is configured to output said address in a first part and a second part, the first part comprising a word address corresponding to the calculated address location in said memory and representing a single memory word and the second part comprising a bit address representing a position of the pixel data within the memory word.

SUB A37

16. The apparatus as claimed in claim 15, further comprising:

a second register for storing said pixel data in said single memory word prior to said word being written to said calculated address location in said memory, said register being capable of storing one memory word; and

a multiplexer for writing data to said register in dependence on said word address or said bit address calculated by said calculation circuit.

17. The apparatus as claimed in claim 16, wherein said multiplexer combines data for two or more pixels to be drawn in dependence on the word address of each of said pixel to permit storage of the data for said two or more pixels in a single memory word.

18. The apparatus as claimed in claim 17, further comprising:

a comparator connected to said calculation circuit for receiving said word addresses, comparing the word addresses of consecutive pixels to be drawn and generating a same address signal if said word addresses are identical.

19. The apparatus as claimed in claim 18, wherein said control circuit is further configured in response to a receipt of said same address signal to control said multiplexer to combine said data for said two or more pixels to be drawn.

20. A method of generating a region of graphics on a display, the method comprising:

(A) receiving X and Y coordinates of a pixel to be drawn in said region;

(B) storing said X and Y coordinates;

(C) calculating an address of a location in a memory for storage of data corresponding to said pixel in dependance on said X and Y coordinates; and

(D) causing said data to be written to and stored in said memory at said address.

21. The method as claimed in claim 20, further comprising:

comparing said X and Y coordinates with predetermined clipping limits and discarding said pixel data in response to said X and Y coordinates exceeding said clipping limits.

SUB A3

22. The method as claimed in claim 20, further comprising:

memory mapping a first register to a first location and a second location in said memory; and

memory mapping a second register to a third location and a fourth location in said memory.

23. The method as claimed in claim 22, further comprising:

monitoring said first, second, third and fourth locations.

24. The method as claimed in claim 23, further comprising:

calculating said memory address for a pixel coordinate in response to one of the following:

a X coordinate being sent to the first register at a preselected one of said first and second locations; and

a Y coordinate being sent to the second register at a preselected one of said third and fourth locations.

25. The method as claimed in claim 20, further comprising:

storing style data corresponding to a predetermined pattern or style for each said pixel;

indexing said style data and generating a style data signal corresponding to said indexed data; and

causing said data to be written to and stored in said memory at said address.

SUB A3

26. A method as claimed in claim 25, further comprising:

selecting a color for said pixel to be drawn in dependence on said style data signal.

27. The method as claimed in claim 20, further comprising:

storing said pixel data in a single memory word prior to a word address word being written to said address in said memory; and

storing said data in said single memory word in dependence on the word address or a bit address.

28. The method as claimed in claim 20, further comprising:

combining data for two or more pixels to be drawn in dependence on a word address of each of said two or more pixels to permit storage of the data for said two or more pixels in a single memory word.

29. The method as claimed in claim 28, further comprising:

comparing the word address of consecutive pixels to be drawn and combining said data for said two or more pixels to be drawn if said word addresses are identical.

ADD A4